# SiGe HBT Technology Development in the DOTSEVEN Project

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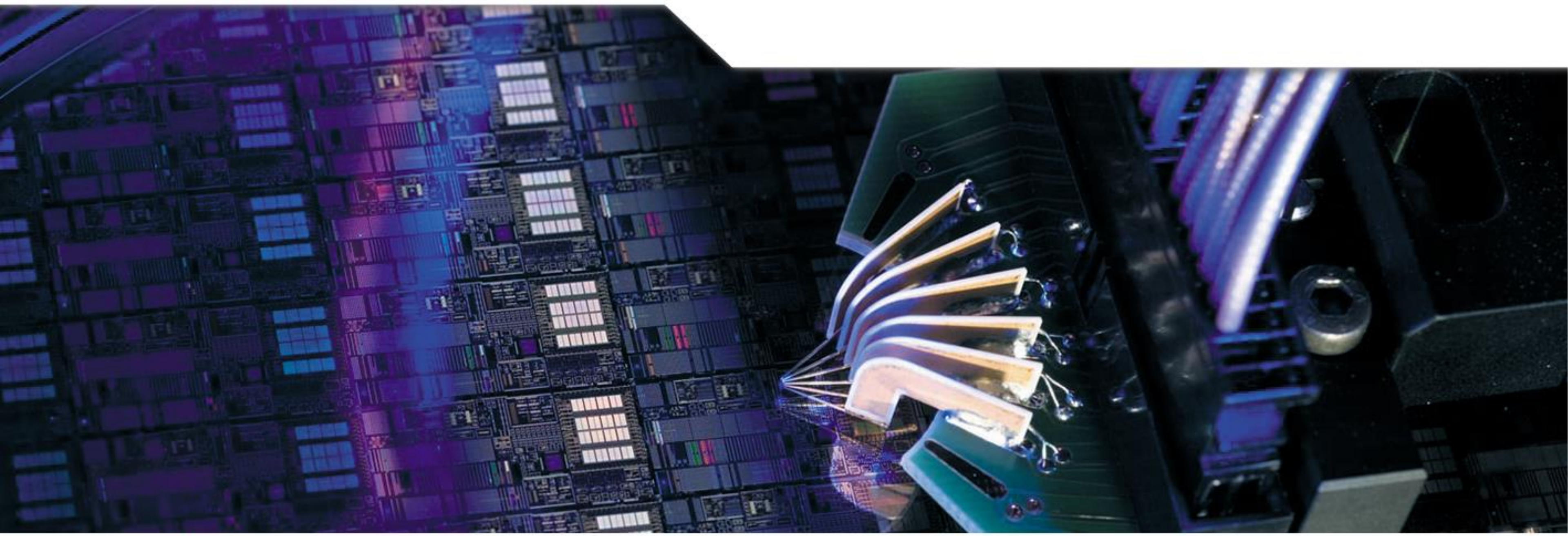
**Open Bipolar Workshop**
**3 October 2013, Bordeaux**



A European Project supported within the Seventh Framework Programme for Research and Technological Development

# Outline

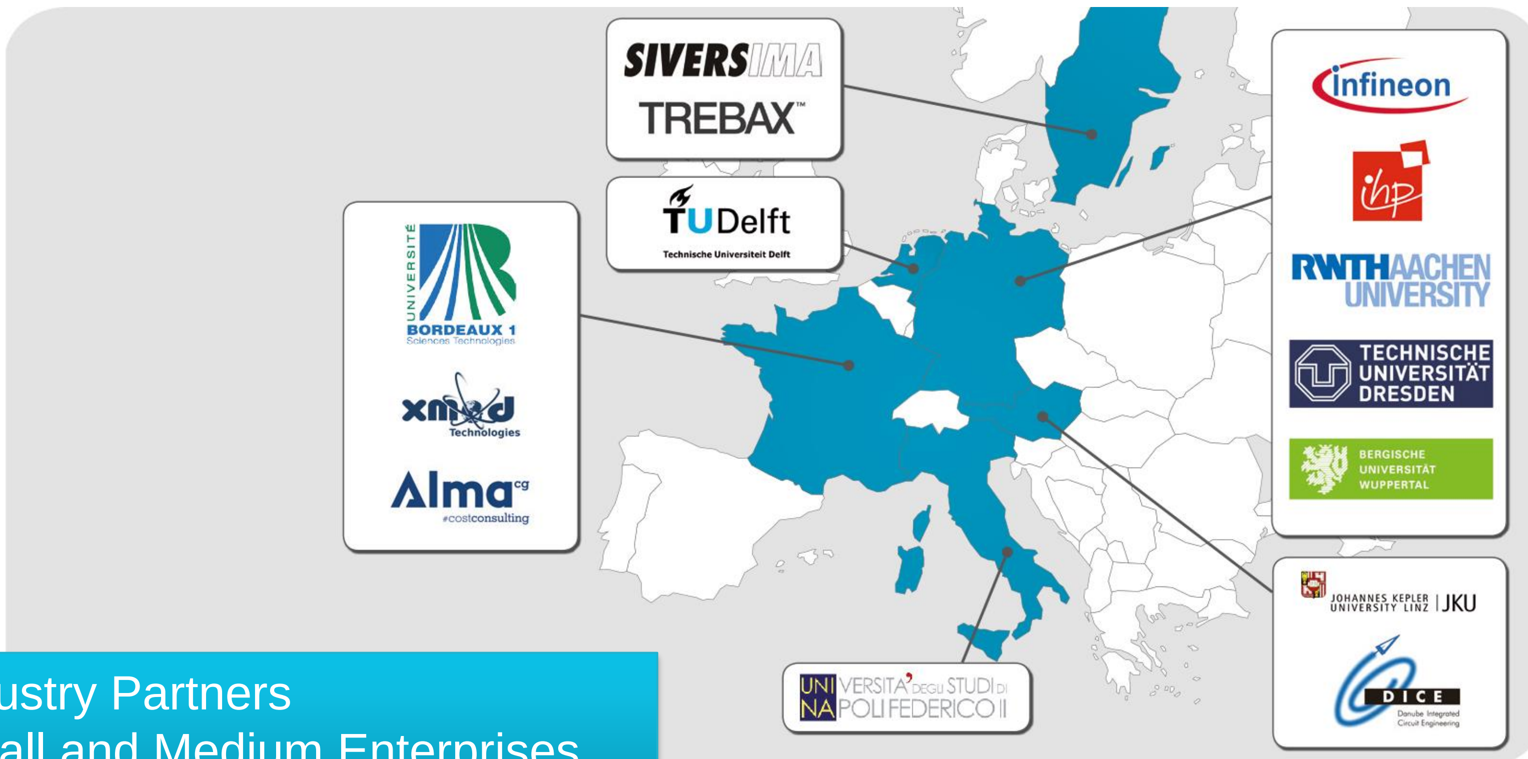
- DOTSEVEN Project
- DOTSEVEN Workpackage 1: SiGe HBT technology platform
  - WP1 - Task 1: Advanced Device Architectures
  - WP1 - Task 2: $F_T$ Enhancement
  - WP1 - Task 3: CMOS Compatibility
  - WP1 - Task 4: Circuit Runs
- Summary

# DOTSEVEN in a Nutshell

- Follows up on successful ideas of DOTFIVE (2/2008 – 7/2011)
- Duration: 10/2012 – 3/2016
- 14 Partners from 6 EU countries
- Project coordinator: Infineon Technologies AG
- Supported by European Commission: FP2 - IP  (ICT 316755)
- Budget: 12.3 M€ (European Commission: 8.6M€)

→ Development of a SiGe HBT technology with $f_{max}$= 700 GHz

# DOTSEVEN Partners




3 Industry Partners
3 Small and Medium Enterprises
8 Academic & Institutional Partners

# Addressed Application Fields

### High-speed Communication

- Broadband ADCs with 50-100GS/s and →25GHz signal bandwidth at 5-6 bit resolution
- 100 Gb/s wireless data transmission
- Satellites

### Radar Applications

- →120 GHz industrial sensors and automation
- Automotive radars (affordable vehicle and road safety for everyone)

### mmWave, THz Imaging and Sensing

- Secure Mass transportation (security screening, mmWave person scanning)
- Heath care and biology
- Medical equipment
- Patient monitoring
- Tissue and genetic screening

# Main Objectives of DOTSEVEN

- The realization of SiGeC Heterojunction Bipolar Transistors (HBTs) operating at a maximum frequency up to 0.7 THz at room temperature

- The design and demonstration of working integrated mm- and sub-mm-wave circuits using such HBTs for specific applications

- The evaluation, understanding, and modeling of the relevant physical effects occurring in such high-speed devices and circuits

# From DOTFIVE to DOTSEVEN

| DOTFIVE Results | | ST [1] | IFAG [1] | IMEC [1] | IHP1 [1] | IHP2 [2] |
|---|---|---|---|---|---|---|
| | $w_E$ | 100 | 130 | 75 | 120 | 155 |
| | $f_T$ | 290 | 240 | 245 | 300 | 310 |
| | $f_{max}$ | **430** | **380** | **460** | **500** | **480** |
| | $BV_{CEO}$ | 1.5 | 1.5 | 1.7 | 1.6 | 1.75 |
| | $\tau_D$ | 1.9 | 2.4 | - | 2.0 | 1.9 |

**RF2THz** 55nm BiCMOS (from ST)

**DOT7** 130nm BiCMOS (B11HFC) (from IFAG)

**DOT7** 130nm BiCMOS (SG13G2) (from IHP1)

**DOT7** EEB-Module (from IHP2)


[1] P. Chevalier et al., “Towards THz SiGe HBTs,” BCTM Tech. Dig., 2011, pp. 57 – 65.

[2] A. Fox et al., “SiGe:C HBT Architecture with Epitaxial External Base,” BCTM Tech. Dig., 2011, pp. 70 – 73.

# Project Organisation: Workpackages (WPs)

- **WP1 : SiGe HBT technology platform**
  - Advanced device architectures
  - $f_T$ enhancement
  - CMOS compatibility
  - Circuit runs
- **WP2 : TCAD and physics-based modeling**
  - Advanced device simulation
  - Development of simulation tools
  - Reliability modeling
- **WP3 : Compact modeling**
  - Parameter extraction & methodology
  - Accurate compact models
  - Predictive & statistical modeling
- **WP4 : Applications & demonstrators**
  - Benchmark circuits
  - MMIC building blocks
  - Application Demonstrators
- **WP5 : Training and dissemination**
- **WP6 : Project management**

# Project Organization: Workpackages (WPs)

| | |
|---|---|
| WP1 : SiGe HBT technology platform | Advanced device architectures<br>$f_T$ enhancement<br>CMOS compatibility<br>Circuit runs |
| WP2 : TCAD and physics-based modeling | Advanced device simulation<br>Development of simulation tools<br>Reliability modeling |
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| WP4 : Applications & demonstrators | Benchmark circuits<br>MMIC building blocks<br>Application demonstrators |
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| WP6 : Project management | |

# WP1 - Task 1: Advanced Device Architectures

**<u>2 Sub–Tasks:</u>**

## (1) Demonstrate 700GHz SiGe - HBT

- Initial HBT architecture: SiGe HBT with epitaxial external base (EEB-module) as developed in DOTFIVE ($f_{max}$ = 480GHz / $\tau_D$ = 1.9ps)

➔ Stage 1: $f_{max}$ = 600GHz / $\tau_D$ = 1.7ps

➔ Stage 2: $f_{max}$ = 700GHz / $\tau_D$ = 1.4ps

## (2) Joint flow IHP/Infineon

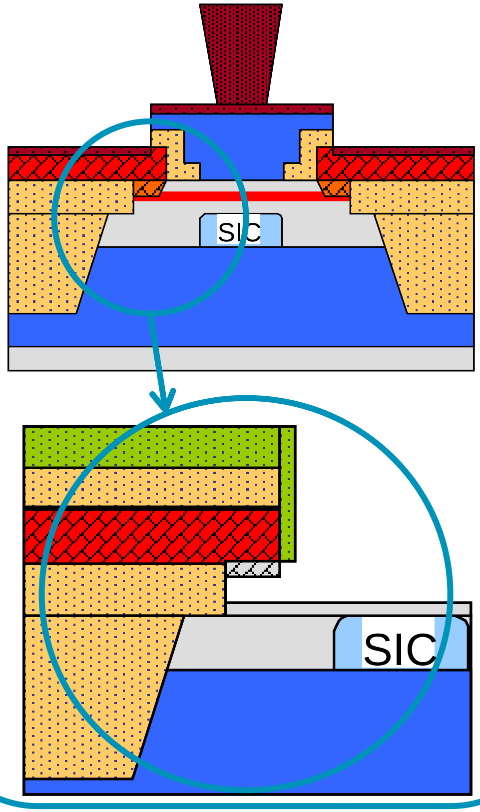
- <u>Pre & post SiGe-HBT processing at Infineon</u> (e.g. shallow- & deep trench / collector epi & implants / resistors for RO / metallization)
- <u>SiGe-HBT module at IHP</u> (architecture with epitaxial external base, EEB)

➔ Demonstrate performance of IHP HBT ($f_{max}$ ~ 500GHz / $\tau_D$ = 1.9ps)

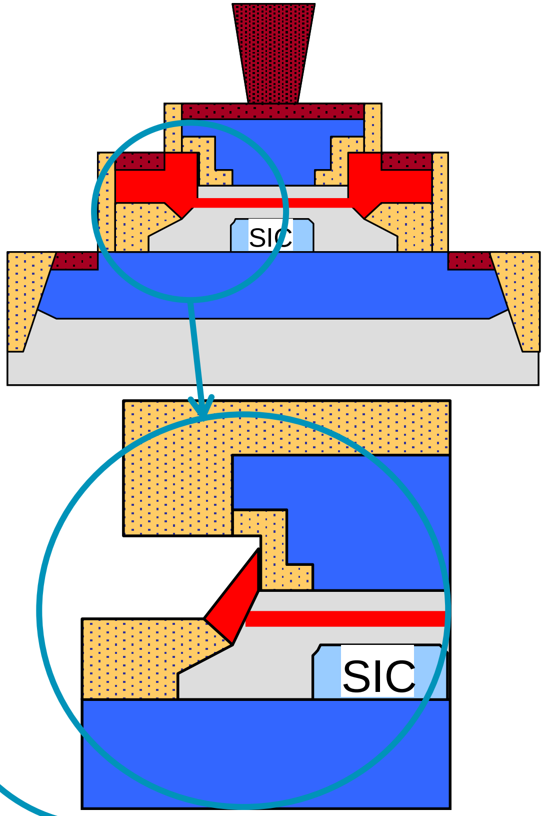
➔ Investigate different collector constructions and metallization schemes

# Review of HBT with Epitaxial External Base (EEB)

Standard DP-SEG HBT




DP-SEG HBT with epitaxial external base (EEB)

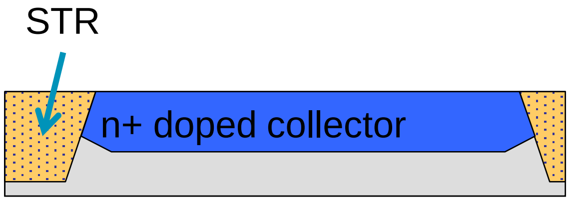



In-situ doped lateral base link growth after SiGe Epi & emitter formation

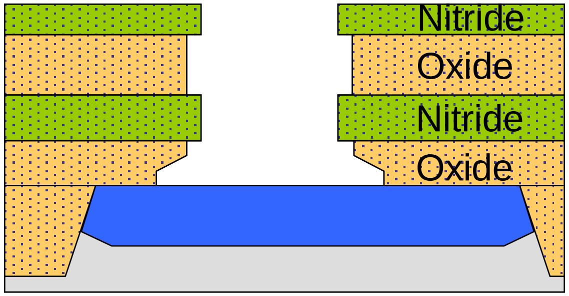
➔ no separate link anneal

➔ lateral link: no compromise $C_{CB}$ vs. $R_B$

# Review of EEB-HBT Process Flow (1/3)

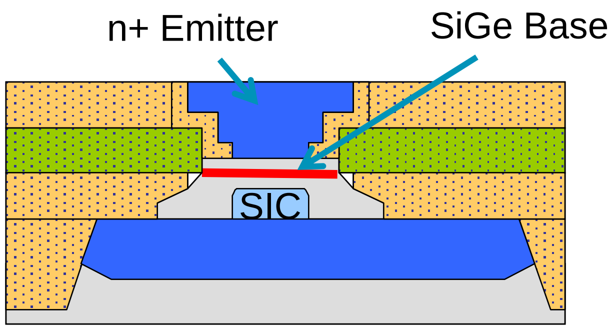



- IHP collector module
  - STR formation
  - Collector implant & anneal

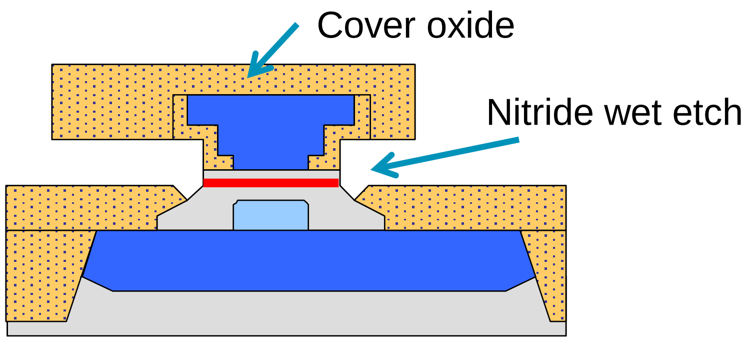



- ONON - Layer stack deposition
- Window dry - etching
- Collector opening by wet - etching

# Review of EEB-HBT Process Flow (2/3)

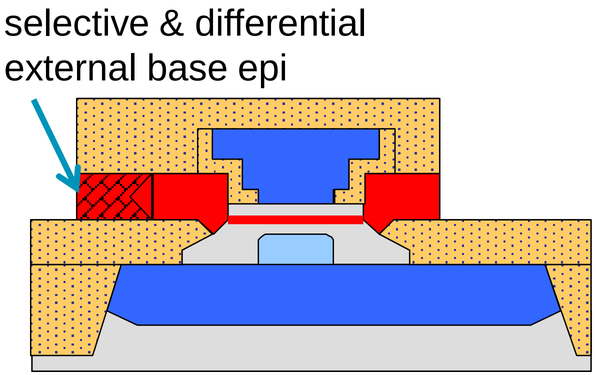



- 2-Step selective epitaxial growth of HBT layer stack (Si-buffer, SiGe-base, Si-cap)
- SIC implant via inside spacers after 1st Si- buffer
- E / B Spacers
- Emitter deposition & CMP

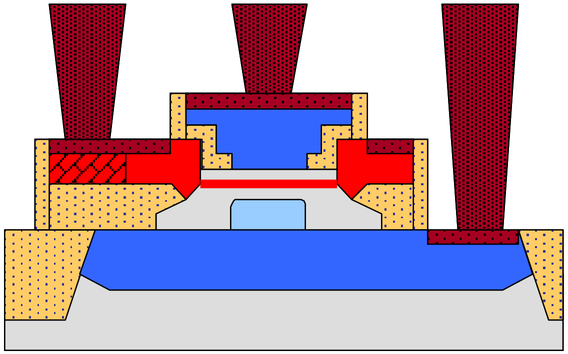



- Cover oxide deposition
- Base patterning
- Nitride removal (wet etching)

# Review of EEB-HBT Process Flow (3/3)

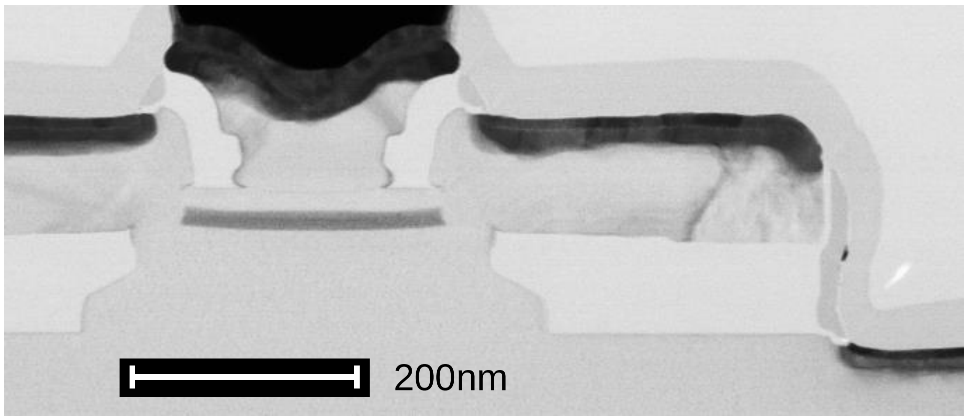


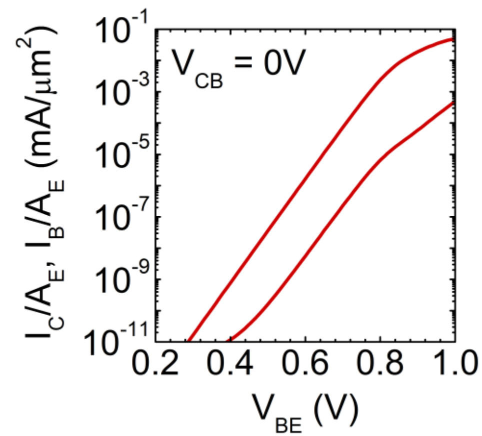

- Selective epitaxial growth of base link
- differential epitaxial growth of outer external base areas
- Si dry-etch via oxide hard-mask

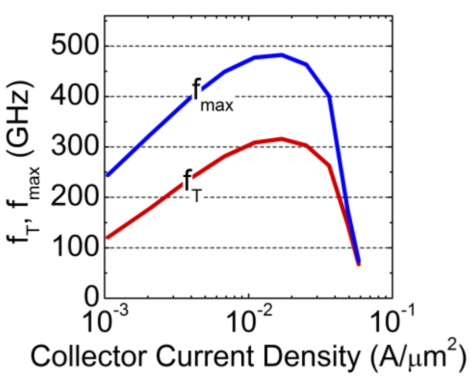


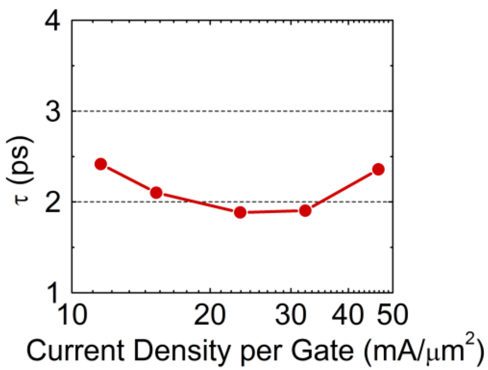
- Oxide removal
- Final RTA
- Silicide formation
- BEOL formation

# Review of DOTFIVE Results for EEB-HBT [1]




| | |
|---|---|
| $W_E$ | 155nm |
| $f_T$ | 310GHz |
| $f_{max}$ | 480GHz |
| $\tau_D$ | 1.9ps |
| $BV_{CEo}$ | 1.75V |
| $\beta$ | 320 |

[1] A. Fox et al., “SiGe:C HBT Architecture with Epitaxial External Base,” BCTM Tech. Dig., 2011, pp. 70 – 73.

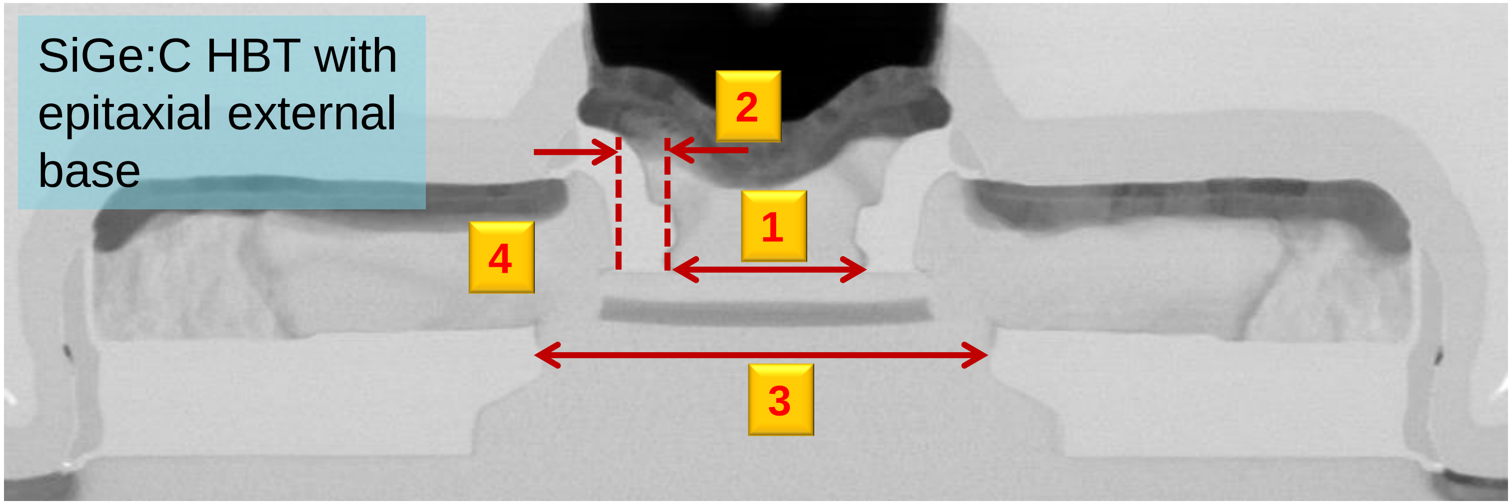
# Subtask 1: Planned EEB-HBT Process Development

- Lateral scaling of different dimensions (see next slide)
- Transfer  layout from 0.25µm to 0.13µm design rules
- Process optimization of external base epitaxy
- Optimize process flow with respect to yield

➔ This is expected to lead to the first stage of performance enhancement

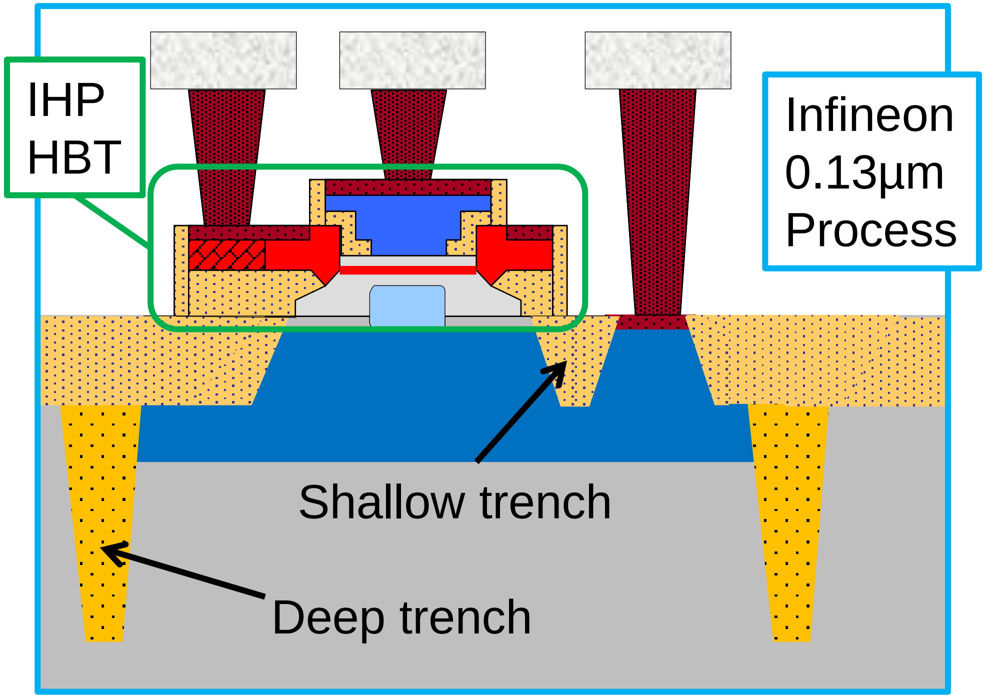
➔ The planning for the second stage will depend on results from this first scaling stage and from results of WP1 - task 2 (vertical profile scaling) and input from WP2 (device simulation) and WP3 (predictive modeling)

# HBT Scaling and Process Adjustment – First Stage




(1) Smaller emitter window (DOTFIVE: 155nm)
(2) Optimize emitter/base spacers: minimum dimension to be explored
(3) Smaller collector window
(4) Process optimization of external base epitaxy

# Task 1 / Sub-Task 2: Joint Flow Infineon & IHP



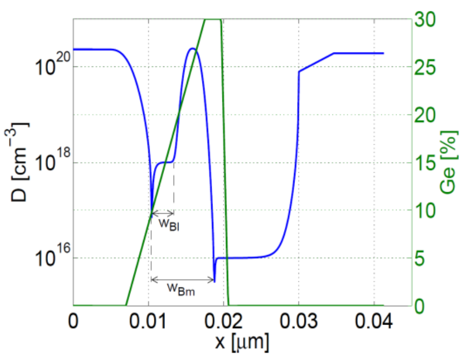

- Joint mask set developed
  - Additional IHP HBT layers in Infineon 0.13µm mask set
  - Layers for IHPs HBT adjusted to Infineons HBT layout
- Process interfaces defined
- Critical processing steps identified:
  - Emitter CMP
  - CVD depositions, incl. SiGe-epitaxy

# WP1 – Task 2: $f_T$ Enhancement

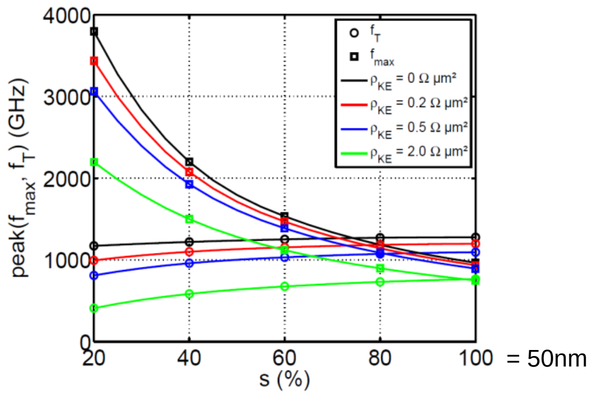
- Advanced simulations predict considerable room for improving $f_T$
  - "Physical limit" beyond 1THz
  - Very aggressively scaled vertical profile
  - Demands on stability at high current densities and emitter resistance very challenging

## Results of Device Simulation [1]

Advanced Profile




Impact of Emitter Resistance




Normalized Emitter Width

CBEBC bulk device

Sef-heating included

Emitter length =10x Emitter width

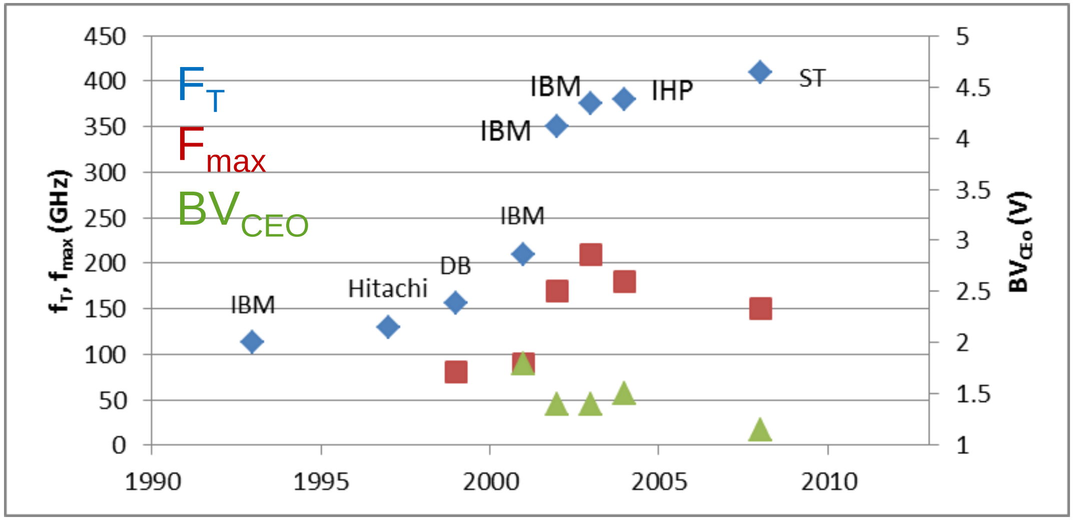
$j_C$@peak $f_T$ > 60mA/µm$^2$ for s=100%

**[1] M. Schröter et al., "Physical and Electrical Performance Limits of High-Speed SiGeC HBTs – Part I and II," IEEE Trans. Electron Devices, vol. 58; No. 11, pp. 3687-3706.**

# Motivation for WP1 Task $f_T$ Enhancement

- Increase of high-speed circuit performance needs balanced improvement of $f_{max}$ and $f_T$
  - Appropriate ratio of $f_{max}/f_T$ needs to be clarified
- How realistic are the predictions?
- How far can $f_T$ be increased under manufacturability constraints?

Development of $f_T$ records for SiGe HBTs




➔ Potential exhausted ?

# Activities for WP1 Task $f_T$ Enhancement

- Develop flow with low-thermal budget for scaling of vertical profile
  - Thermal treatments >650°C shall be avoided before final RTP step
- Optimize base profile on technology with non-selective base-epitaxy
  - More flexibility for generating extreme profile variations
- Platform for device model parameter calibration
  - Fabrication of HBTs with special base profiles for validating device simulations
- Impact of back-end processes have to be investigated
- First studies for $f_T$ maximization don't need further lateral scaling
  - Only in 2nd project phase test of optimized vertical profiles in flows with low external parasitics

# WP1 – Task 3: CMOS Compatibility

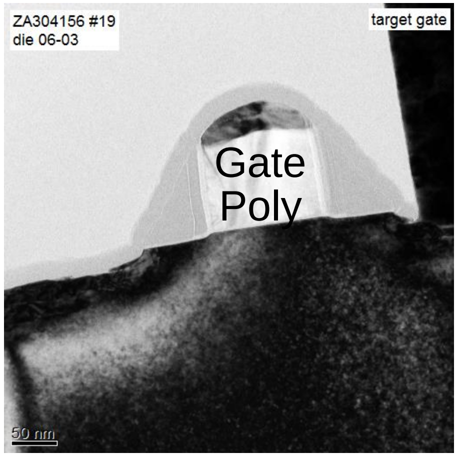
- DOTFIVE: pure bipolar technology developed
  - Suitable for applications like 60GHz WLAN or 77GHz radar
- Future product generations require more digital functionality
  - E.g. memory, interfaces, A/D conversion and base band processing

➔ BiCMOS integration will be investigated in DOTSEVEN

- Integration of the conventional (DPSA-) SiGe HBT developed in DOTFIVE into a 130nm CMOS platform at Infineon
- Investigation of possibility to adapt IHP’s HBT with epitaxially grown base link to Infineon’s 130nm BiCMOS platform
- IHP SG13G2

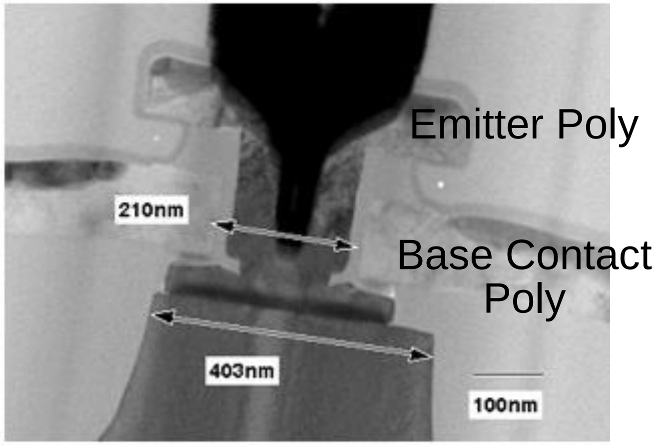
# Technology Concept B11HFC (Infineon)

130nm MOSFETs
(C11)



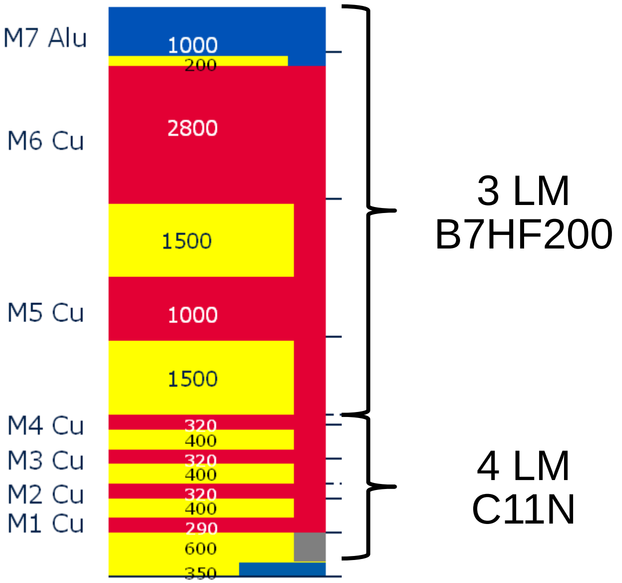

+

Scaled SiGe HBTs
(DOTFIVE SiGe HBT)




+

mmWave
BEOL




0.13 µm SiGe BiCMOS with 7 layer BEOL

# Constrains of HBT Integration into CMOS

- General constraint for BiCMOS development in practice:
  - HBT is integrated into an established CMOS technology
    ➔ CMOS devices should not be changed (reuse CMOS IP, ROM, SRAM, …)
  - MOS thermal steps (LDD-, SD-anneals, poly oxidation) deteriorate HBT performance

- Three problems were identified for integration of DOTFIVE HBT into Infineon‘s 130nm CMOS technology

  (1) Wafer orientation for best HBT performance and yield (notch in [010] orientation) is different from CMOS standard

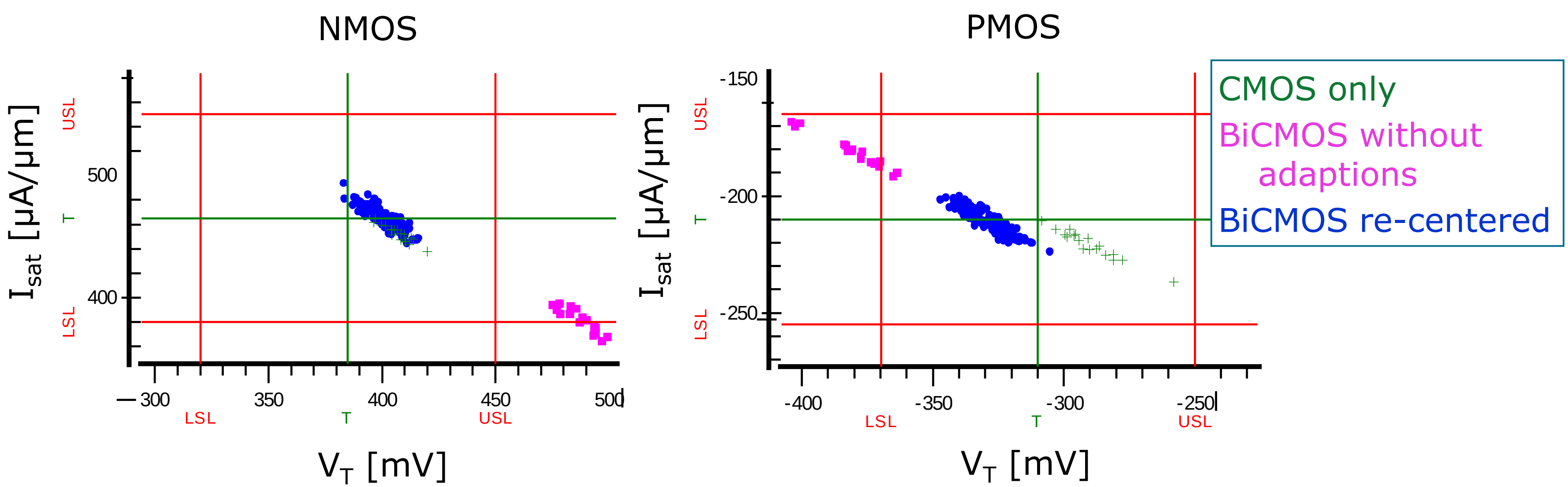
  (2) Incompatible thermal budgets for HBT and CMOS fabrication

  (3) Structural problems during process integration

# CMOS Integration Problems: Corrective Measures

- (1) Substrate orientation: adjust CMOS
  - Re-center MOS parameters by modification of implant and anneal steps
- (2) Thermal budget: find compromise
  - Reduce LDD anneal so that the MOS-parameters can still be re-centered and the base can be deposited before CMOS spacers
  - Reduce S/D anneal so that MOS parameters can still be re-centered
  - Adjust base- and emitter-modules of the HBT to the reduced S/D anneal (which is still higher than in the DOTFIVE HBT process)
- (3) Structural problems: manifold!
  - Example: removal of layers of bipolar fabrication from MOS-gates → introduction of a nitride protection layer that acts as etch-stop-layer during layer removal

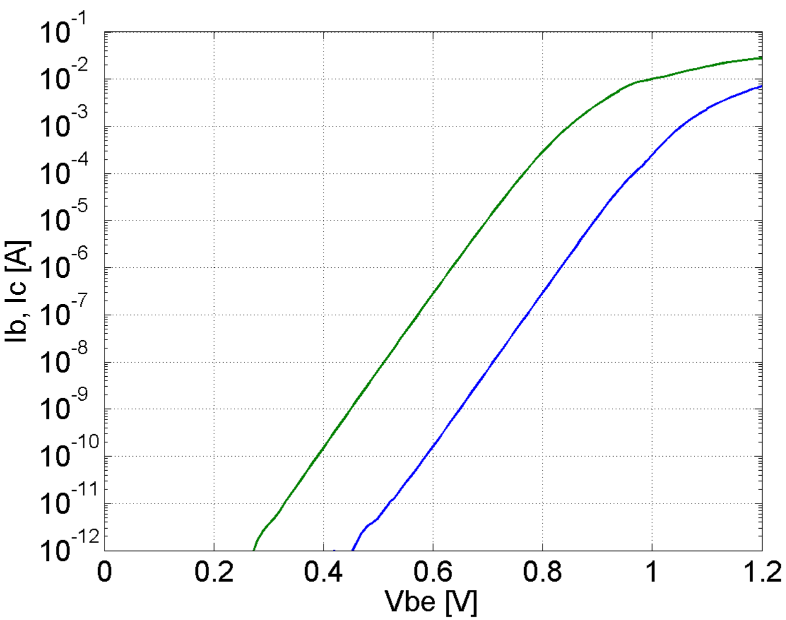
# Re-Centering of CMOS: LDD and SD Implants

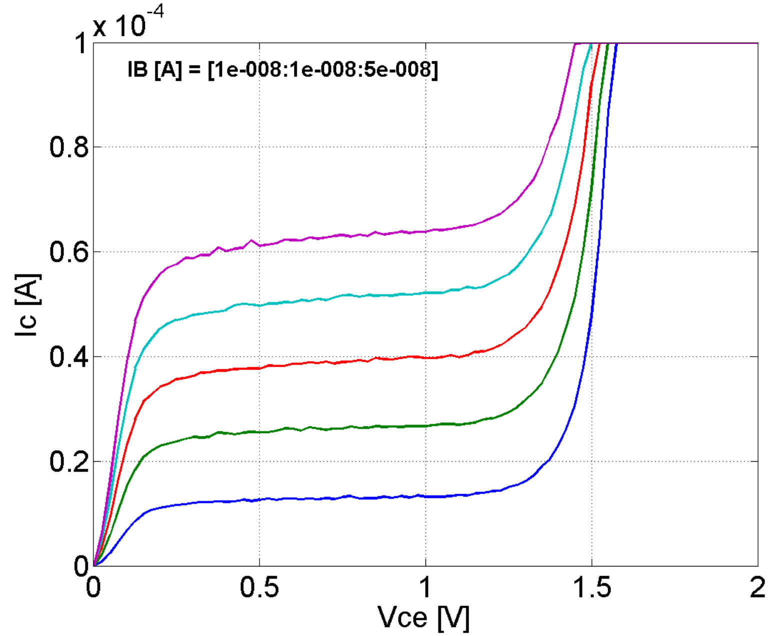



- Modified substrate orientation
- Modified thermal budget
- NMOS re-centered
- PMOS re-centered with respect to current
  - Improved leakage due to rotated substrate

| | CMOS | BiCMOS |
|---|---|---|
| Notch | 0° | 45° |
| LDD anneal | 1006°C, 5 sec. | 1010°C spike |
| S/D anneal | 1006°C, 5 sec. | 1050°C spike |

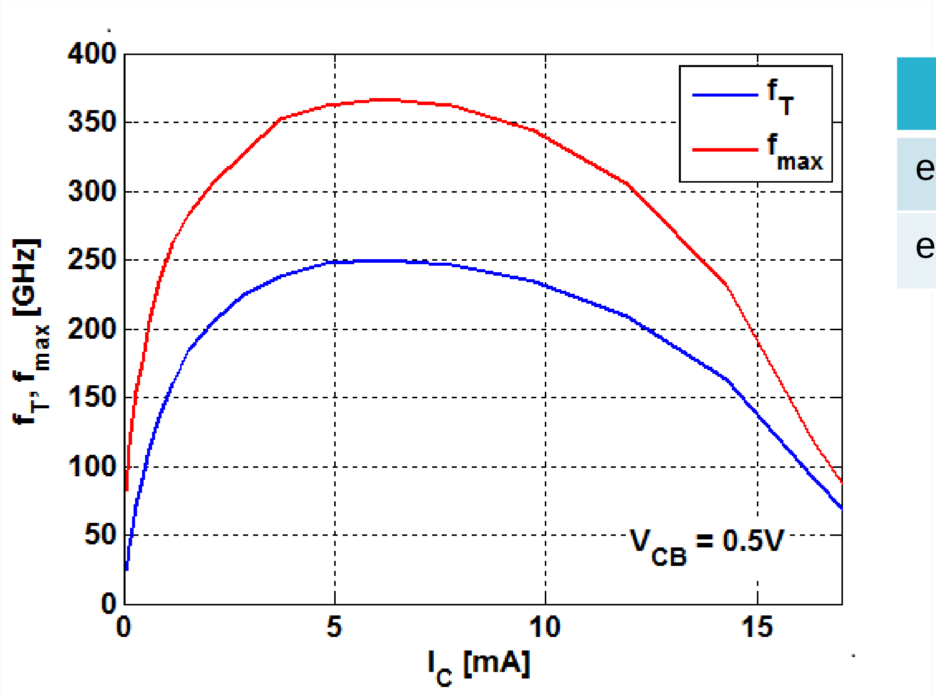
# DC Characteristics of SiGe HBT in BiCMOS Flow




- Successful integration of DOTFIVE SiGe HBT with 0.13 µm CMOS
- Adjusted emitter doping to enable emitter drive-in with CMOS S/D anneal
- Ideal transfer characteristics with very low base leakage current

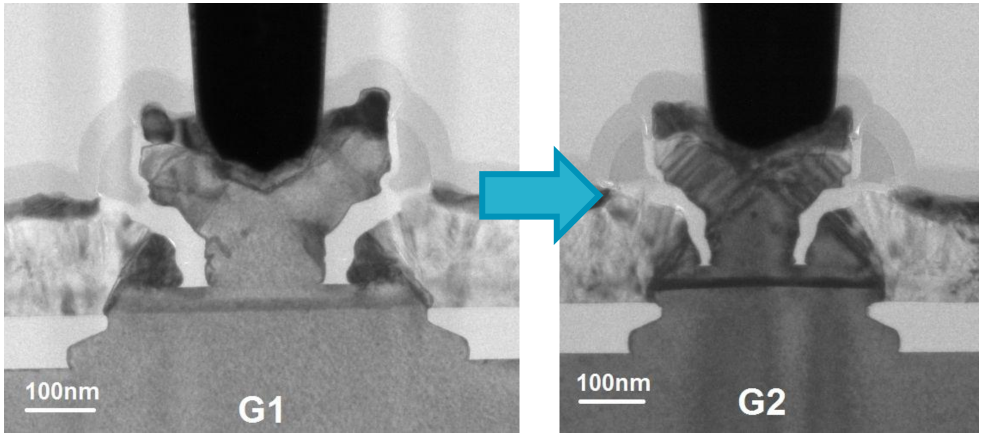
# RF Performance SiGe HBT in BiCMOS Flow

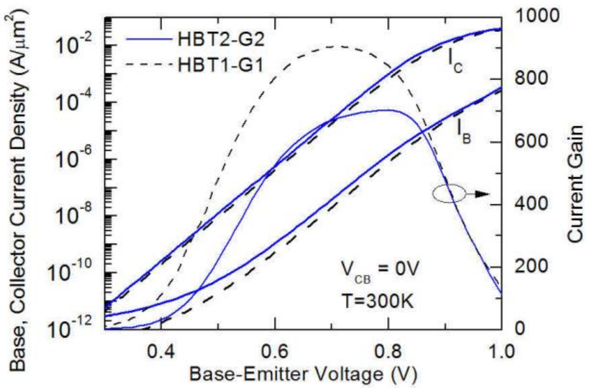


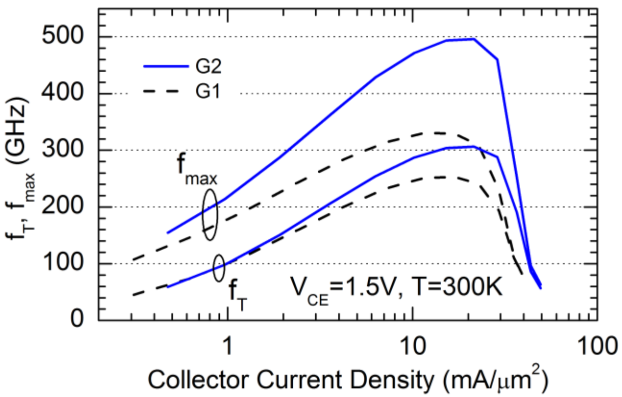

| | DOTFIVE | BiCMOS |
|---|---|---|
| emitter doping | 2 x $10^{21}$ $cm^{-3}$ | 3 x $10^{20}$ $cm^{-3}$ |
| emitter drive-in | 930°C, 3 sec. | 1050°C spike |

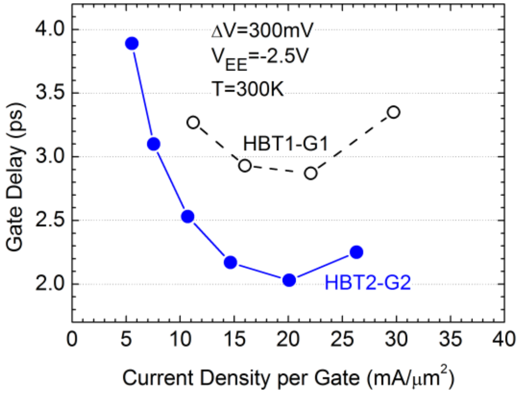
- Adjusted emitter doping to enable emitter drive-in with CMOS S/D anneal
- 250 GHz $f_T$, 360 GHz $f_{max}$
- Similar performance in BiCMOS flow as in pure bipolar (DOTFIVE)

# SG13G2: IHPs 130nm BiCMOS + DOTFIVE HBT [1]



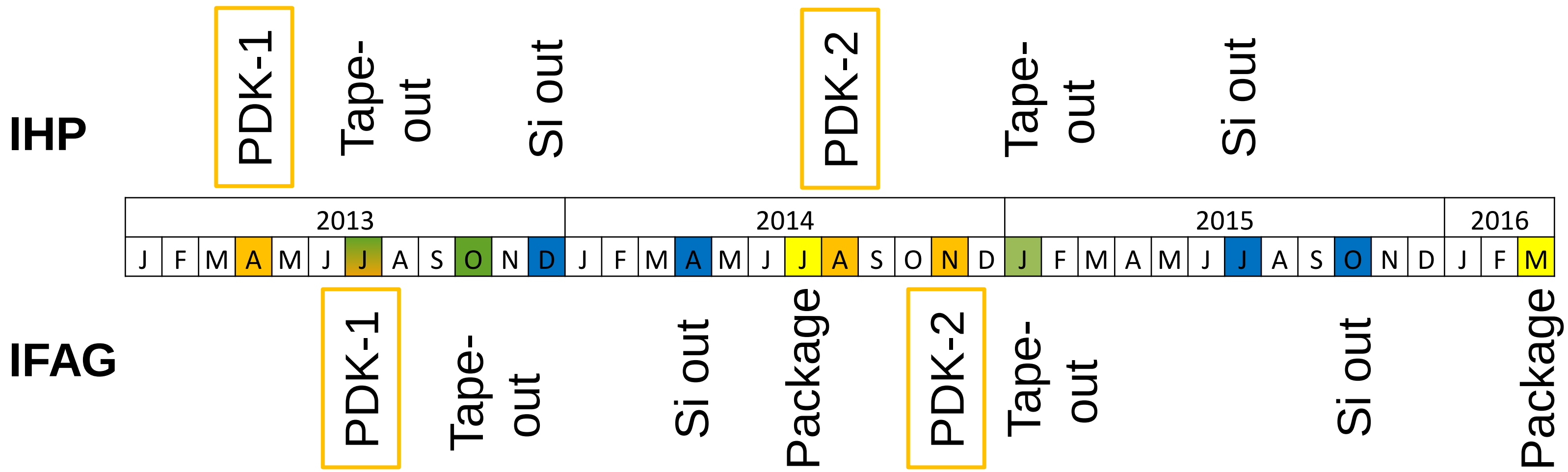




| | G1 | G2 |
|---|---|---|
| $w_E$ (nm) | 170 | 120 |
| $f_T$ (GHz) | 250 | 300 |
| $f_{max}$ (GHz) | 330 | 500 |
| $\tau_D$ (ps) | 2.9 | 2.0 |
| $BV_{CEo}$ (V) | 1.6 | 1.6 |
| β | 900 | 700 |


[1] H. Rücker et al., SIRF 2012, Santa Barbara, USA, pp. 133 – 136

# WP1 – Task 4: Circuit Fabrication



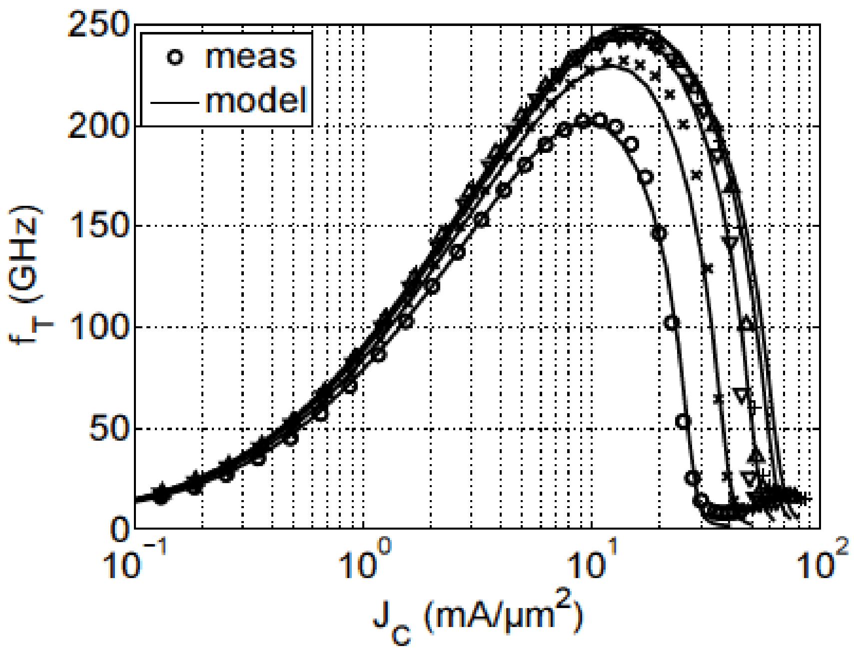

- Two complete circuit fabrication cycles at Infineon and IHP
- Infineon additionally provides package runs
- The first iteration of PDKs is based on the DOTFIVE technologies
- The second iteration of PDK's will include technology advancements, as far as yield and stability can be ensured

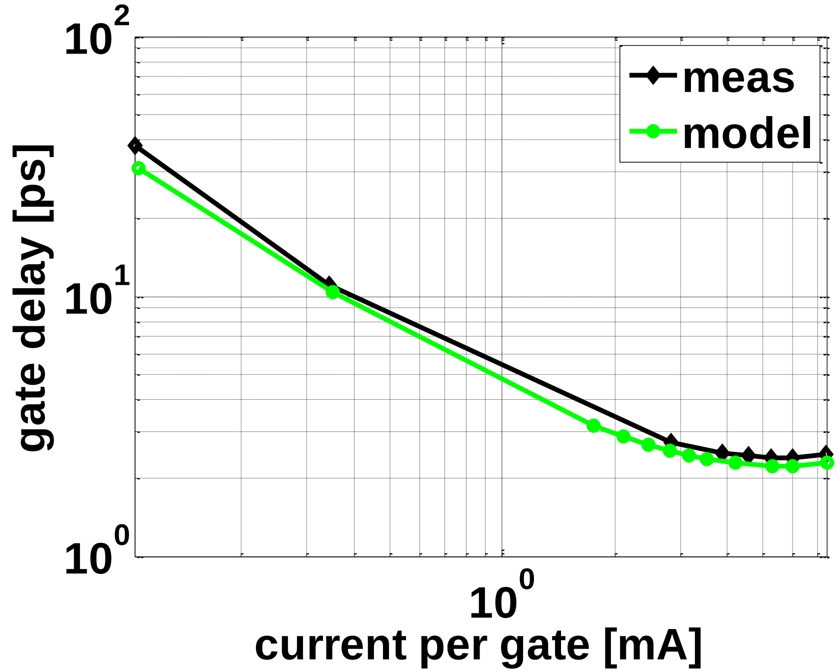
# Infineon Process Design Kit for First Design Cycle

- Process B11HFC: 130nm BiCMOS process with latest DOTFIVE HBT performance level
- PDK including the required simulation models, layout cells, and verification tools (DRC, LVS, …) delivered to the circuit partners
- Comprehensive library of scalable npn transistors for optimizing applications (emitter length range of 0.7µm to 10.0µm, different contact configurations like BEC, BEBC, CBEBC, …)
- TaN resistor, MIM capacitor, high-performance varactor (based on the high voltage npn transistor), transmission lines, …
- Physics-based compact models, including advanced HiCUM models for the high speed npn transistors by TU Dresden

# Infineon Process Design Kit for First Design Cycle

- Examples for model / hardware correlations on device and circuit level

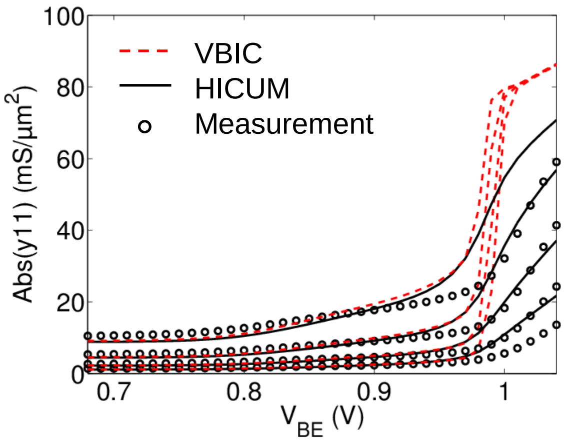


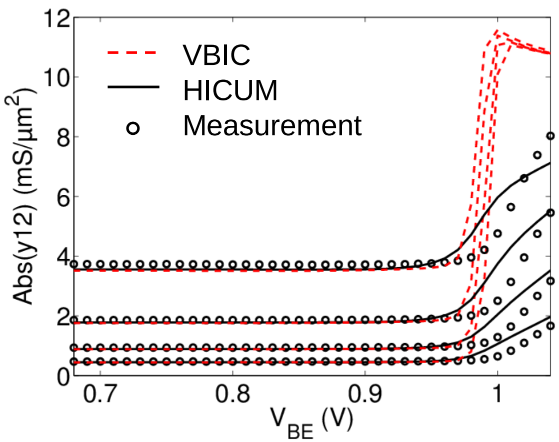




HiCUM model vs. measurements for (a) $f_T$ vs collector current (@ $V_{CB}$ from -0.5 to +0.5V) and (b) CML ring oscillator gate delay.

# IHP Process Design Kit for First Design Cycle

- Process SG13G2: 130nm BiCMOS process with latest DOTFIVE HBT performance level
- HICUM Model introduced to IHP design-kit
- VBIC Model with improved substrate network
- Symmetric MOS varactors introduced to IHP PDK




HICUM fits Y-parameters in the high current regime better than VBIC

# Summary

- HBTs with $f_{max}$ = 700GHz / $\tau_D$ = 1.4ps and circuit demonstrators operating up to 240GHz are targeted for Q1 2016
- In the first step improvements up to $f_{max}$ = 600GHz/$\tau_D$ = 1.7ps are expected by scaling the HBT architecture with epitaxial external base (EEB) developed in DOTFIVE
- Industry compatibility of the EEB architecture will be tested in a joint flow between Infineon and IHP
- $f_T$ limits will be explored by testing aggressive vertical profiles
- Investigate BiCMOS integration issues of advanced SiGe HBTs
- Two complete design cycles by both technology partners are scheduled for demonstration of integrated mm- and sub-mm-wave circuits

# Acknowledgement


- Andreas Pawlack, Julia Krause (TU Dresden, HiCUM modelling)
- Holger Rücker (IHP)